REMARKS

The Office Action dated July 9, 2003, has been received and carefully noted. The amendments made herein and the following remarks are submitted as a full and complete response thereto.

Claims 1, 7, 9 and 10 have been amended, and claim 8 has been cancelled without prejudice. New claims 11 and 12 have been added. Applicants submit that the new claims as well as the amendments made herein are fully supported in the specification and the drawings as originally filed, and therefore no new matter has been added. Accordingly, claims 1-7 and 9-12 are pending in the present application and are respectfully submitted for consideration.

Claims 5-7 and 10 were rejected under 35 U.S.C. § 102(b) as being anticipated by Imura et al. (U.S. Patent No. 5,398,212, hereinafter "Imura"). Applicants respectfully submit that each of claims 5-7 and 10 recites subject matter that is neither disclosed nor suggested by the cited prior art.

Claim 5 recites a semiconductor memory device having a plurality of memory cells corresponding to an address space larger than 2^n and smaller than $2^{(n+1)}$, where n is a positive integer, an invalid address detecting circuit for detecting that an address signal supplied from exterior indicates an address space other than the address space, and an output controlling circuit for outputting. When the invalid address detecting circuit carries out the detection in a read operation, a data signal read in a read operation cycle immediately precedes the read operation.

Accordingly, at least one of the essential features of the present invention is "an output controlling circuit for outputting, when said invalid address detecting circuit

carries out said detection in a read operation, a data signal read in a read operation cycle immediately preceding said read operation." As such, the present invention results in the advantage of invalidating an operation cycle in the case where an invalid address signal has been received during the cycle.

It is respectfully submitted that the prior art fails to disclose or suggest the elements of the Applicants' invention as set forth in claims 5-7 and 10, and therefore fails to provide the advantages which are provided by the present application.

Imura discloses a semiconductor memory device having a memory cell array 3 with $(2^n +m)$ memory cells. The n and m are integers satisfying the relationship $2^n < 2^n +m < 2^n +1$. An address buffer circuit 1 and an address decoder 2 of Imura function to specify one of the memory cells included in the memory cell array 3 in accordance with an address signal of (n+1) bits (A_0 to A_n). The address buffer circuit 1 is an input interface circuit for converting the address signal of A_0 to A_n on an address bus into an address signal for an internal logic level. The converted address signal is supplied to the address decoder 2. The address decoder 2 decodes the address signal, and selects one of the memory cells included in the memory cell array 3. Data for D_0 to D_i which is stored in the selected memory cell is amplified by a sense amplifier and thereafter is output through an output buffer circuit 4. The output buffer circuit 4 is an output interface circuit for outputting the data of D_0 to D_i which is read out from the memory cell array 3 to a data bus.

Applicants respectfully submit that each and every element recited within claim 5 is neither disclosed nor suggested by Imura. In particular, Applicants submit that the semiconductor memory device as recited in the present application is clearly distinct

from that which is illustrated by the cited prior art. Specifically, it is submitted that the cited prior art fails to disclose or suggest at least the limitation of "an output controlling circuit for outputting, when said invalid address detecting circuit carries out said detection in a read operation, a data signal read in a read operation cycle immediately preceding said read operation."

It is submitted that Imura merely shows a non-empty address is accessed after detecting an empty address. On the other hand, present invention provides that a read operation is not carried out when an address is detected as an empty address (p. 10, lines 15-18 of the present application), and provides that the read data, having been accessed and read in advance, is outputted. In addition, semiconductor memory device of the present invention is neither comparable nor analogous to that which is shown in Imura because the circuit as described in col. 6, lines 52-54 of Imura requires a circuit for converting the received empty address into a non-empty address, and requires additional time-delay for making the address conversion. Accordingly, Applicants submit that Imura fails to disclose each and every element recited in claim 5 of the present applicant, and therefore is allowable.

As for claim 6, it is submitted that claim 6 depends from independent claim 5. Therefore, Applicants submit claim 6 is also allowable due to its dependency from independent claim 5.

As for the rejection of claims 7 and 10, it is submitted that claims 7 and 10 have been amended to reflect a new dependency. Claim 7 has been amended to depend on independent claim 1, and claim 10 has been amended to depend on independent claim 9. Thus, the rejection with respect to claims 7 and 10 will be addressed below.

Claims 1-4, 8 and 9 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Imura in view of Howard (U.S. Patent No. 5,754,816). In making this rejection, the Examiner cited Imura for disclosing substantially all of the claimed elements of the present invention with the exception of showing the invalid signal outputting circuit for outputting an invalid signal to the exterior when the invalid address detecting circuit carries out the detection. Howard was cited for allegedly curing this deficiency. Applicants respectfully submit that each of claims 1-4, 8 and 9 recites subject matter that is neither disclosed nor suggested by the cited prior art.

Claim 1 recites a semiconductor memory device having a plurality of memory cells corresponding to an address space larger than 2^n and smaller than $2^{(n+1)}$, where n is a positive integer, an invalid address detecting circuit for detecting that an address signal supplied from exterior indicates an address space other than the address space, and an invalid signal outputting circuit for outputting an invalid signal to the exterior of the semiconductor memory device when the invalid address detecting circuit carries out the detection, thereby notifying a system unit accessing the semiconductor memory device of the detection.

Claim 9 recites a method of controlling a semiconductor memory device having a plurality of memory cells corresponding to an address space larger than 2^n and small than $2^{(n+1)}$, where n is a positive integer. The method includes the step of outputting an invalid signal to exterior of the semiconductor memory device when an address signal supplied from the exterior indicating an address space other than the address space has been detected, thereby notifying a system unit accessing the semiconductor memory device of the detection.

Howard discloses a data memory in which data words having access control bits and further bits are stored at each memory location 34. When a particular memory location is addressed of Howard, then the access control bits stored at that memory location are output to control logic 12, 46 that serves to generate a valid access signal. The valid access signal of Howard is fed back to the selected memory location and controls whether the further bits stored at that memory location are output. If access to those further bits is not permitted by the access control bits, then the further bits are not output and power is saved. The control logic of Howard is responsive to hardware and software flags in addition to the access control bits.

Applicants respectfully submit that each and every element recited within claims 1 and 9 is neither disclosed nor suggested by Imura and/or Howard, taken alone or in combination. In particular, Applicants submit that the semiconductor memory device and the method controlling thereof as recited in the present application is clearly distinct from that which is illustrated by the combination of the cited prior art. Specifically, it is submitted that the cited prior art fails to disclose or suggest at least the limitations of "an invalid signal outputting circuit for outputting an invalid signal to the exterior of the semiconductor memory device when the invalid address detecting circuit carries out the detection, thereby notifying a system unit accessing the semiconductor memory device of the detection" and "the step of outputting an invalid signal to exterior of the semiconductor memory device when an address signal supplied from the exterior indicating an address space other than the address space has been detected, thereby notifying a system unit accessing the semiconductor memory device of the detection."

It is submitted that the Examiner admits that Imura fails to disclose or suggest the limitation of "the invalid signal outputting circuit for outputting an invalid signal to the exterior when the invalid address detecting circuit carries out the detection" as recited in the claimed invention. Furthermore, Applicants submit that Howard fails to cure the deficiencies which exist in Imura because Howard fails to show or describe outputting the valid access signal output from the control logic to the system unit controlling the data storage apparatus. Therefore, the combination of Imura and Howard is neither comparable nor analogous to the present invention. Specifically, it is submitted that the combination of cited art fails to provide a system unit that can easily recognize that the invalid address signal has been supplied to the semiconductor memory device. Accordingly, Applicants submit that neither Imura and/or Howard, taken alone or in combination, disclose or suggest each and every element recited in claims 1 and 9 of the present application, and therefore is allowable.

As for claims 2-4, it is submitted that each of claims 2-4 is dependent on independent claim 1. As such, each of claims 2-4 is allowable due to its dependency on allowable claim 1.

As for claim 8, Applicants submit that the rejection with respect to claim 8 is now moot since claim 8 has been canceled without prejudice.

With regard to claims 7 and 10, it is submitted that claims 7 and 10 are dependent on independent claims 1 and 9, respectively. As such, each of claims 7 and 10 is allowable due to its dependency on allowable claims 1 and 9, respectively.

As for new claims 11 and 12, it is submitted that each of claims 11 and 12 is dependent on independent claim 1. As such, each of claims 11 and 12 is allowable due to its dependency on allowable claim 1.

In view of the above, Applicants respectfully submit that Claims 1-7 and 9-12, each recites subject matter that is neither disclosed nor suggested in the cited prior art. Applicants also submit that the subject matter is more than sufficient to render the claims non-obvious to a person of ordinary skill in the art, and therefore respectfully request that claims 1-7 and 9-12 be found allowable and that this application be passed to issue.

If for any reason, the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact the Applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper has not been timely filed, the Applicants respectfully petition for an appropriate extension of time. Any fees for such an extension, together with any additional fees that may be due with respect to this paper, may be charged to counsel's Deposit Account No. 01-2300, **referencing docket number 108397-00011.**

Respectfully submitted,

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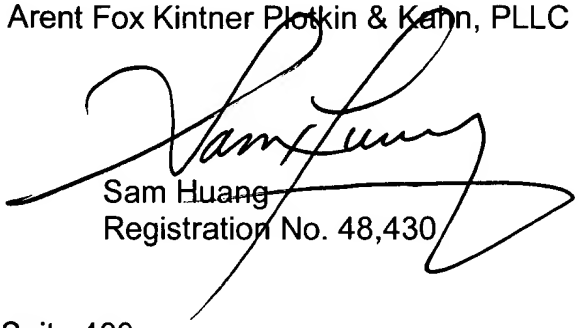

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